Journal of
Electrical & Electronic Systems

Vadodaria et al., J Electr Electron Syst 2015, 4:2
DOI: 10.4172/2332-0796.1000154

Research Article Open Access

Design and Implementation of High Gain, High Unity Gain Bandwidth, High Slew Rate and Low Power Dissipation CMOS Folded Cascode OTA for Wide Band Applications

Vadodaria MU*, Patel R and Popat J

Department of Electrical Engineering, Marwadi Education Foundation's, Rajkot-Morbi Road, Gujrat, India

Abstract

A novel differential input pair and single output OTA is designed in this paper. This FCOTA is designed by using current mirror and its enhanced gain parameter and also is reduce the power dissipation and increase the gain bandwidth. Simulation results are performed using Mentor Graphics software model for CMOS TSMC 180 nm process technology. The supply voltage is given 1.8 v. The designed FCOTA has different capacitive load and according its Gain, Unity Gain Bandwidth, Power Dissipation, Phase Margin and Slew Rate are measured. Gain, Unity Gain Bandwidth and Slew Rate are optimizing up to 97.37 db, 20.83 GHz and 3.5075 KV/μs respectively. The power dissipation reduces up to 8.31 μW. This FCOTA is designed for wide band application because of high gain and high bandwidth and low power dissipation.

Keywords: Folded cascode structure; Current mirror; Gain; Unity gain bandwidth; Power dissipation; Slew rate

Introduction

Amplifier is one of the basic and important circuits which have a wide range of applications in sever. This is accomplished by the continual integration of complex analog building blocks on a single chip [1]. Gain and Speed both are most important parameter in amplifier. Power dissipation is most important factor in any analog circuit. Designing high-performance base band analog circuits is still a hard task to reduced power consumption and increased frequency and gain [2]. Current tendency focus on some radio-software receivers which suppose a RF signal conversion after the antenna [3]. Thus, a very higher sampling frequency and resolution analog-to-digital converter design is required. Folded Cascode OTA is a solution of Telescopic Cascode OTA. There have some limitations of the voltage swing. To remove the drawback of telescopic OTA i.e. limited output swing and difficulty in shorting the input and output a Folded Cascode OTA is used. This design follows three stages such as (i) Input Pair, (II) Current mirror Cascode Stage and (III) Biasing Stage. Current mirror is a one type of approach to copy current at output side [4].

Design Approach

One way of increasing the impedance is to add some MOSFETs at the output side or in second stage to include for using an active load. MOSFETs are stacked on top of each other. The MOSFETs are called "cascode", and will increase the output impedance and thereby increase the gain [5]. Here in this cascode pair, there is given self biasing using current mirror. The current mirror is one of the main parts of the most analogue and mixed-signal integrated circuits to copy current such as OTAs [5,6].

Here the Figure 1 is consisting of M1 and M2 is called Current Mirror. In the current mirror channel length modulation is neglecting.

$$I_{ref} = \mu_n C_{ox} \left(\frac{W}{L}\right)_1 \left(V_{gs} - V_{th}\right)$$

$$I_{ref} = \mu_n C_{ox} \left(\frac{W}{L}\right)_2 \left(V_{gs} - V_{th}\right)$$

So, take ratio of the I_{out} and I_{ref} $g_{m1} = G_{m1}$

$$r_{08}$$

$$I_{out} = \frac{(W/L)2}{(W/L)1} I_{ref}$$

Constructing the bias circuit of an amplifier to provide the required bias current [7]. Transistor trans-conductance is the most important parameters in amplifier that must be stabilized. In general biasing of an amplifier is to ensure the proper operation of the circuit.

Design Analysis

This schematic design is consisting of three stages. First stage is NMOS input pair, second stage is cascode stage and third stage is biasing circuit. The input stage is designed by N-MOS input pair. Due to the greater mobility of NMOS device, PMOS input differential pair has a lower transconductance than carrier a NMOS pair. Thus, NMOS MOSFET has been chosen to ensure the largest gain required. For a folded OTA bandwidth performance is high. So here N-MOS input pair is applied for high transconductance. So as shown in Figure 2 M1 and M2 are NMOS input pair MOSFETs.

MOSFETs M1 and M2 are input pair of the OTA. M11 transistor work as a load register of NMOS pair. Second Stage is the Cascode OTA with current mirror or it's also called current mirror biasing.

Cascode stage design for higher isolation at input and output side, higher input impedance, higher output impedance, higher gain and higher bandwidth. So (M3, M4), (M5,M6) are NMOS pair and (M7,M8), (M9,M10) are PMOS pair are working as a current mirror self biased. Third stage is biasing circuit. The width of the M12 is low because if the width of M13 is higher the internal resistor value will

***Corresponding author:** Vadodaria MU, Department of Electrical Engineering, Marwadi Education Foundation's, Group of Institutions, Rajkot-Morbi Road, Gujrat, India, Tel: +91- 7874128777; E-mail: vadodaria.maulik91@gmail.com

Received June 06, 2015; **Accepted** August 12, 2015; **Published** August 30, 2015

Citation: Vadodaria MU, Patel R, Popat J (2015) Design and Implementation of High Gain, High Unity Gain Bandwidth, High Slew Rate and Low Power Dissipation CMOS Folded Cascode OTA for Wide Band Applications. J Electr Electron Syst 4: 154. doi:10.4172/2332-0796.1000154

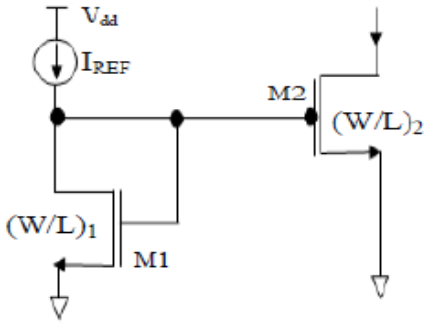

Figure 1: Basic Current Mirror.

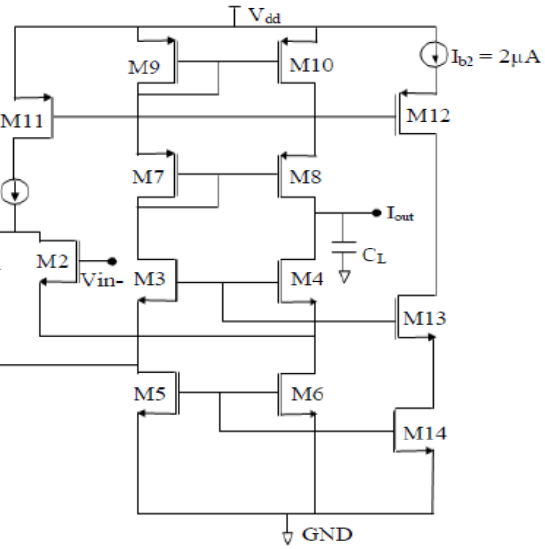

Figure 2: Folded Cascode OTA using Current Mirror Self Biasing.

be low and its gate terminal is directly connected to the M11, which is work as a PMOS load resistor.

$$g_{ml} = \mu_n C_{ox} \left(\frac{W}{L}\right)_1 \left(V_{gs} - V_{th}\right)$$

And internal resistance is defined by R_{out}

$$R_{out} = (g_{m8} r_{08} r_{10}) \,||\, (g_{m4} r_{04} r_{08})$$

So, Voltage gain A_v

$$A_v = G_{m1} R_{out}$$

$$A_v = g_{m1} R_{out}, \text{ where, } g_{m1} = G_{m1}$$

Internal resistance of M8 is represent as r_{08} and it's defined as

$$r_{08} = \frac{1}{\lambda I_{d8}}$$

Where, λ is channel length modulation and I_{d8} is the drain current.

$$I_{d8} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_8 \left(V_{gs} - V_{th}\right)^2$$

There are two poles exits and it is denoted by P1 and P2

$$P_1 = \frac{1}{R_{out} C_L}$$

$$P_2 = \frac{1}{R_{08} C_L}$$

Where $R_{08} = g_{m8} r_{08} \left(2 r_{08} \,||\, r_{10}\right)$

According to mathematical calculation, there are minor changes in mathematical calculation and theoretical calculation. Now, there is present waveform of FCOTA's schematic.

Performance Parameter

Table 1 presents different sizes of MOSFETs according to its operation.

Table 2 represents the summary of proposed performance parameter using 180 nm technology. There are different capacitive load such as 1 pF. 2 pF and 5.6 pF.

Simulation Result

All simulation results are measured by using 180 nm or 0.18_m technology using Mentor Grphics-Pyxis (Figures 3-6).

Conclusion

A novel design of Folded Cascode Operational Transconductance Amplifier (FCOTA) using current mirror as self biasing and biasing of the driving stage has been presented in this research work. The proposed design of FCOTA has been simulated and analyzed using Mentor Graphics tools. Improvement in performance parameters such as Gain up to 97.36 db, UGB up to 20.83 GHz , Reduction in Power Dissipation is 8.31 W and Slew Rate enhanced upto 3.5075 KV/µs has been achieved with respect to reference papers designs. So this FCOTA is designed for low power, high gain and high UGB. And it's used for wide band applications.

MOSFETs	Width (µm)	MOSFETs	Width (µm)
M1	14	M8	20
M2	14	M9	21
M3	5	M10	21
M4	5	M11	21
M5	5	M12	7
M6	5	M13	5
M7	14	M14	5

Note : All MOSFETs's length is fixed L = 0.18 µm.

Table 1: Size of MOSFETs.

Parameters	CL=1pF [1]		CL=2pF [2]		CL=5.6pF [3]	
	CFC	PFC	CFC	PFC	CFC	PFC
Gain (db)	58.37	97.37	59	97.37	68.48	97.36
Gain Margin(db)	N.A	14.89	N.A	20.86	N.A	29.77
Phase Margin (°)	62.5	38.32	86	55.66	26.3	79.51
UGB	315 MHz	20.83 GHz	86.1 MHz	12.7 GHz	247.1 MHz	5.25 GHz
Slew Rate	N.A	3.5075 KV/µs	N.A	3.5075 KV/µs	92.8V/S	3.5075 KV/µs
Power Dissipation	540 µW	8.31 µW	750 µW	8.31 µW	2.943 mW	8.31 µW

Note: CFC = Conventional Folded Cascode

Table 2: Performance parameter.

Figure 3: 1 pF Capacitive Load.

Figure 4: 2 pF Capacitive Load.

Figure 5: 5.6 pF Capacitive Load.

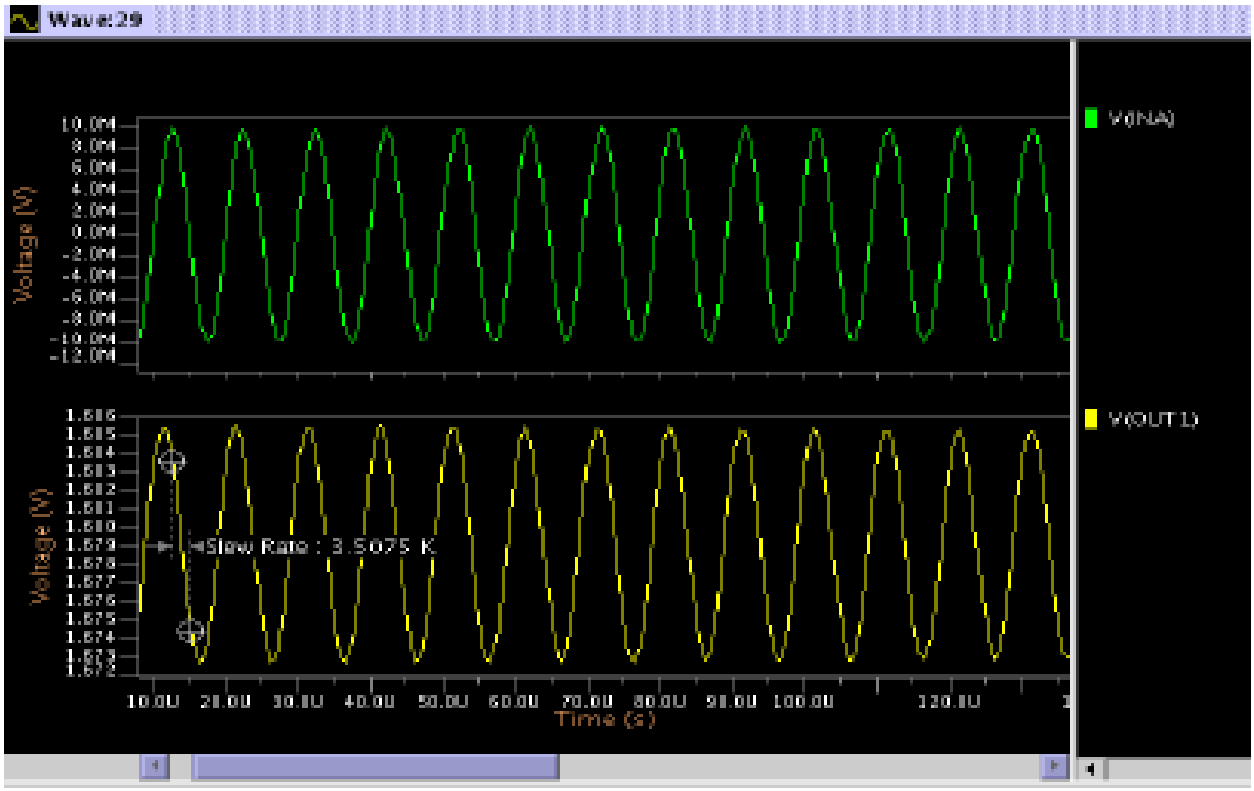

Figure 6: Slew Rate.

References

1. Biabanifard S, Akbari M, Asadi SM, Yagoub CE (2014) High performance folded cascode OTA using positive feedback and recycling structure, School of Electrical Engineering and Computer Science, University of Ottawa, Canada.
2. Patra P, Jha PK, Dutta A (2013) An Enhanced Recycling Folded Cascode OTA with a Positive Feedback, IEEE.
3. Daoud H, Salem BS, Zouari S, Loulou M (2006) Folded Cascode OTA Design for Wide Band Applications, Information technologies and electronic laboratory, LETI National engineers school of Sfax, IEEE, Tunisia.
4. Akbari M, Nazari M, Javid A (2014) Enhancing Phase Margin of OTA using Self Biasing Cascode, Laboratory, Shahid Beheshti University, GC, Iran.
5. Patra P, Jha PK, Dutta A (2013) An Enhanced Recycling Folded Cascode OTA with a Positive Feedback, IEEE.
6. Razavi B (2000) CMOS Circuit design, layout and simulation, professor of electrical engineering University of California, McGraw-Hill Publication, Los Angeles.
7. Daoud H, Salem BS, Zouari S, Loulou M (2006) Folded cascode OTA design for wide band applications, information technologies and electronic laboratory, LETI National engineers school of Sfax, IEEE, Tunisia.